AMENDMENTS TO THE CLAIMS

1. (Cancelled)

2. (Currently Amended) A semiconductor device comprising:

a die having:

a semiconductor structure that includes a substrate and a plurality of device regions formed in ~~and over a~~ the substrate, the device regions being conductive; and

an interconnect structure that contacts the semiconductor structure, and forms a top surface of the die, the interconnect structure including:

a dielectric structure; ~~and~~

a plurality of layers of metal that are formed in and isolated by the dielectric structure, each metal layer having a plurality of metal traces that are electrically connected to the device regions; and

a plurality of bond pads that touch the dielectric structure, the plurality of bond pads being electrically connected to a plurality of metal traces; and

a conductive region ~~formed over~~ having a bottom surface adhered to only a non-conductive region of the top surface of the die above the plurality of layers of metal, the conductive region including silicon and being spaced apart from the plurality of bond pads.

3. (Cancelled)

4. (Currently Amended) The semiconductor device of claim 2 and further comprising:

a first ~~via~~ conductive structure that makes an electrical connection with ~~a region of~~ a metal trace and a first end of the conductive region; and

a second ~~via~~ conductive structure spaced apart from the first conductive structure that makes an electrical connection with ~~a region of~~ a metal trace and a second end of the conductive region.

5. (Currently Amended) The semiconductor device of claim 4 wherein the ~~conductive region~~ silicon has a concentration of dopant atoms.

6. (Original) The semiconductor device of claim 2 and further comprising:

a dielectric region formed to contact the conductive region; and

a conductor region formed to contact the dielectric region.

7. (Currently Amended) The semiconductor device of claim 6 and further comprising:

a first ~~via~~ conductive structure that makes an electrical connection with ~~a region of~~ a metal trace and the conductive region; and

a second ~~via~~ conductive structure spaced apart from the first conductive structure that makes an electrical connection with ~~a region of~~ a metal trace and the conductor region.

8. (Currently Amended) The semiconductor device of claim 7 wherein the ~~conductive region~~ silicon has a concentration of dopant atoms.

9. (Original) The semiconductor device of claim 2 wherein the dielectric structure includes a plurality of layers, including an overlying passivation layer, the conductive region being formed over the passivation layer.

10. (Currently Amended) The semiconductor device of claim 9 and further comprising:

a plurality of contacts formed in the dielectric structure, the contacts electrically connecting the device regions to the metal traces that are formed from a first layer of metal; and

a plurality of vias formed in the dielectric structure, the vias electrically connecting vertically adjacent metal traces and regions~~; and~~

~~a plurality of pads formed in the dielectric structure, the pads being connected to a number of vias to form external points of electrical connection~~.

Claims 11-22 (Cancelled)

23. (Currently Amended) A semiconductor device comprising:

a die having:

a semiconductor structure that includes a substrate and a plurality of conductive regions formed in ~~and near a~~ the substrate; and

an interconnect structure having a top surface, and a bottom surface that contacts the semiconductor structure, the interconnect structure having:

a dielectric structure,

a plurality of metal interconnects formed within the dielectric structure, the metal interconnects making electrical connections with the plurality of conductive regions, and

a test structure ~~that contacts the top surface, the test structure~~ including ~~a capacitor;~~ :

~~a first opening formed in the dielectric structure, the first opening extending from the top surface down to a first region on a metal interconnect; and~~

~~a first conductive structure formed in the first opening to make an electrical contact with the first region, and on the top surface to make an electrical connection with the test structure~~

a first conductive region having a first surface adhered to an exterior surface of the interconnect structure and an opposing second surface;

an insulation region having a first surface and an opposing second surface, the first surface of the insulation region contacting the second surface of the first conductive region; and

a second conductive region having a first surface and an opposing second surface, the first surface of the second conductive region contacting the second surface of the insulation region, the second conductive region being electrically isolated from the first conductive region.

24. (Cancelled)

25. (Currently Amended) The semiconductor device of claim 23 and further comprising:

a first opening formed in the dielectric structure, the first opening extending from the top surface down to a first region on a metal interconnect;

a first conductive structure formed in the first opening to make an electrical connection with the first region, and on the top surface to make an electrical connection with the test structure;

a second opening formed in the dielectric structure, the second opening extending from the top surface down to a second region on the metal interconnect; and

a second conductive structure formed in the second opening to make an electrical ~~contact~~ connection with the second region, and on the top surface to make an electrical connection with the test structure.

Claims 26-27 (Cancelled)

28. (Currently Amended) ~~The semiconductor device of claim 25 and further comprising~~ A semiconductor device comprising:

a die having:

a semiconductor structure that includes a substrate and a plurality of conductive regions formed in the substrate; and

an interconnect structure having a top surface, and a bottom surface that contacts the semiconductor structure, the interconnect structure having:

a dielectric structure,

a plurality of metal interconnects formed within the dielectric structure, the metal interconnects making electrical connections with the plurality of conductive regions, and

a test structure that contacts the top surface;

a first opening formed in the dielectric structure, the first opening extending from the top surface down to a first region on a metal interconnect;

a first conductive structure formed in the first opening to make an electrical connection with the first region, and on the top surface to make an electrical connection with the test structure;

a second opening formed in the dielectric structure, the second opening extending from the top surface down to a second region on the metal interconnect;

a second conductive structure formed in the second opening to make an electrical connection with the second region, and on the top surface to make an electrical connection with the test structure; and

a third opening formed in the dielectric structure, the third opening extending through the metal interconnect to break an electrical connection between the first and second regions of the metal interconnect.

29. (Currently Amended) A semiconductor device comprising:

a die having:

a semiconductor structure having a substrate and a plurality of device regions formed in the substrate, the device regions being conductive; and

an interconnect structure that contacts the semiconductor structure, the interconnect structure having:

a dielectric structure; ~~and~~

a plurality of metal interconnects formed within the dielectric structure, the metal interconnects making electrical connections with the plurality of device regions, and

a plurality of bond pads that touch the dielectric structure, the plurality of bond pads being electrically connected to a plurality of metal traces; and

a test device ~~formed on~~ having a bottom surface adhered to only a non-conductive region of an exterior surface of the die, the test device including a region of silicon and being spaced apart from the plurality of bond pads.

30. (Currently Amended) The semiconductor device of claim 29 and further comprising:

a first ~~via~~ conductive structure that is electrically connected to a device region and a first end of the test device; and

a second ~~via~~ conductive structure that is electrically connected to a device region and a second end of the test device.

31. (Previously Presented) The semiconductor device of claim 30 wherein the region of silicon has a concentration of dopant atoms.

32. (Previously Presented) The semiconductor device of claim 29 and further comprising:

a dielectric region formed to contact the region of silicon; and

a conductor region formed to contact the dielectric region.

33. (Previously Presented) The semiconductor device of claim 32 and further comprising:

a first ~~via~~ conductive structure that is electrically connected to a device region and the region of silicon; and

a second ~~via~~ conductive structure that is electrically connected to a device region and the conductor region.

34. (Previously Presented) The semiconductor device of claim 33 wherein the region of silicon has a concentration of dopant atoms.

35. (New) The semiconductor device of claim 28 wherein the test device includes a first conductive region having a first surface adhered to an exterior surface of the interconnect structure and an opposing second surface.

36. (New) The semiconductor device of claim 35 wherein the test device includes an insulation region having a first surface and an opposing second surface, the first surface of the insulation region contacting the second surface of the first conductive region.

37. (New) The semiconductor device of claim 36 wherein the test device includes a second conductive region having a first surface and an opposing second surface, the first surface of the second conductive region contacting the second surface of the insulation region, the second conductive region being electrically isolated from the first conductive region.